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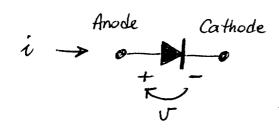
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CLASS NOTES

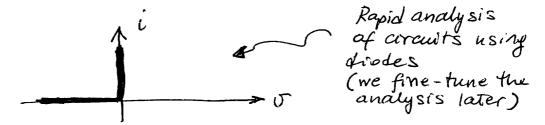
CHAPTER 5

The diode is a non linear device. It has a non linear i-v characteristic.

It exhibit a behavior which is dependent on the direction of the applied voltage.

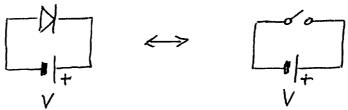


The ideal disde



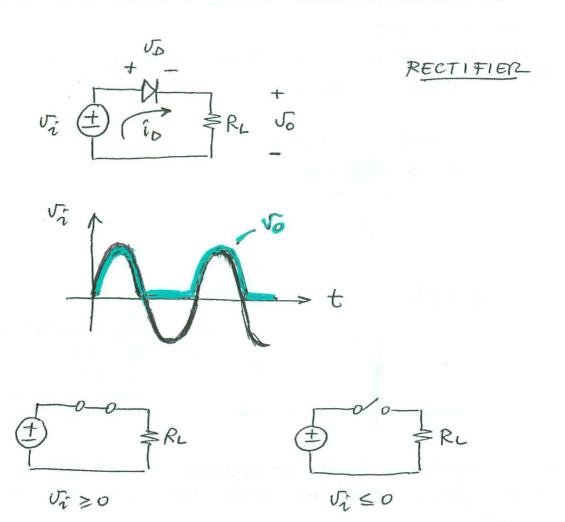
if a negative voltage is applied to the diode, no current flows and the diode behaves like an open circuit.

A diode operated in the reverse direction (reverse brased) is said to be CUT OFF.

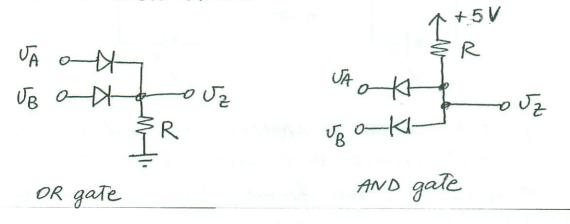


If a positive voltage is applied the ideal diode behave like a short circuit and current flows through it. A diode eperated in the forward direction (forward biased) is said to be <u>ON</u>.

let's see a couple of interesting ways we could use a circuit element with such a behavior:



DIODE LOGIC GATES:



Diode current-voltage characteristic

Theoretical analysis of a pn junction results in the following i-v relationship:

$$\hat{i} = I_S \left(e^{\sigma/\eta V_T} - 1 \right)$$

$$V_T = \frac{KT}{9}$$
 = thermal voltage { at room temperature
 $27^{\circ}C (= 300^{\circ}K)$ the
 value of $V_T = 26 \text{ mV}$

 $K = Boltzmann's constant = 1.38 \times 10^{-23}$ joules | kelvin T = temperature in kelvin = 273 + temperature in C q = magnitude of electron charge = 1.6 $\times 10^{-19}$ Coulomb $\gamma = empirical$ scaling constant = exponential ideality factor Ts = saturation current

 η has a value between $0.5 \div 2$. It depends on the material (type of semiconductor used and the doping). In general we will assume $\eta = 1$ unless otherwise specified

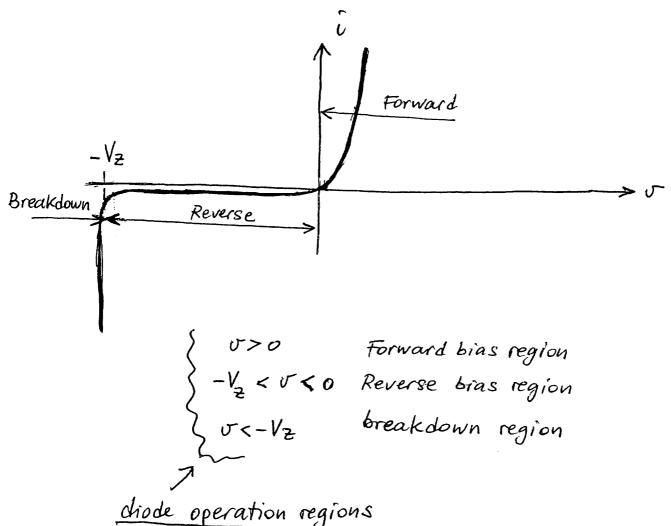
Is is sometime called scalle factor. That's because it is directly proportional to the cross-sectional area A of the diode. Thus doubling the junction area results in a diode with double the value of Is and as the diode equation indicates, double the value of current i.

The value of Is is of the order of 10-15 A however is a very strong function of temperature.

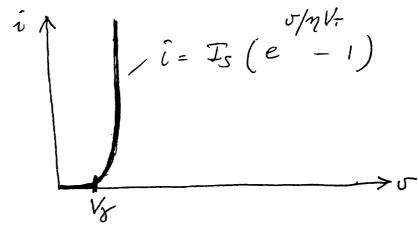
The parameter of the volt-ampere characteristic:

A plot of Logis versus Jo results in a straight line of slope 0-434 from which y is obtained.

IN4153 -> 722



diode operation regions



A glance at the i-v characteristic in the forward region reveals that at room temperature the current is negligibly small for v smaller than about 0.6 V.

This value by is usually referred as cut-involtage. or threshold voltage.

Typical values of the threshold voltage (at room temperature) for different commonly used semiconductors are;

silicon $\Rightarrow V_{\gamma} = 0.6V$ germanium $\Rightarrow V_{\gamma} = 0.2V$ gallium arsenide $\Rightarrow V_{\gamma} = 1.2V$

If we operate at room temperature and apply forward voltages we can reasonably assume that;

$$i = I_s (e - 1) \approx I_s e$$

$$\frac{5/\eta V_T}{\rho} = \frac{5/\eta V_T}{\rho}$$
 $i = I_s (e - 1) \approx I_s e$

$$\frac{5/\eta V_T}{\rho} = \frac{5/\eta V_T}{\rho}$$
 $v = v = (\ln 10) V_T = 2.30.26 \text{ mV} \approx 52 \text{ mV}$

For voltages less than by the curve can be approximated by a straight line of slope close to o.

Since the slope (1/80) is the conductance that means that the conductance is very small in this region =) the resistance is very high

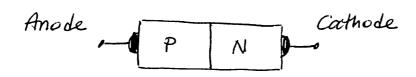
For voltages above of the curve can be approximated by a straight line with a very large slope. The conductance is therefore very large the equivalent resistance is very small

$$g_{d} = \frac{di_{D}}{dv_{D}} = \frac{d}{dv_{D}} \left(\overline{I}_{S} e^{-\overline{I}_{S}} \right) = \overline{I}_{S} \frac{d}{dv_{D}} \left(e^{-\overline{I}_{S$$

$$G = \frac{1}{gd} = \frac{\eta V_T}{\hat{v}_D + \bar{I}_S}$$

- DYNAMIC RESISTANCE Usually not all the voltage applied at the diode terminals appears at the p-n junction there is a small drop due to the ohmic contact resistance between the metallic terminals and the semiconductor

Pd + Contact - DIODE RESISTANCE



Forward dynamic resistance

$$r_d = \frac{\gamma V_T}{\hat{c}_D + \bar{I}_S} \approx \frac{\sqrt{mV_T}}{\hat{c}_D}$$

$$\hat{c}_D >> \bar{I}_S$$

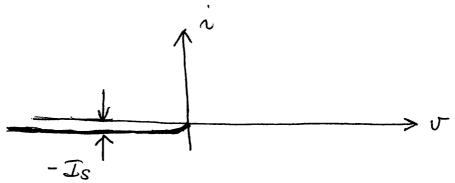
Reverse Region

The reverse bias region is entered when the diode voltage or is made repative.

If v is negative and few times larger than 4 in magnitude the exponential term becomes negligibly small compared to unity and we can reasonably write that:

$$\hat{i} = \bar{I}_{S} \left(e^{-1} \right) \approx -\bar{I}_{S}$$

$$e^{\sigma/\eta V_{T}} \ll 1$$



This mean that;
The current in reverse direction is approximately constant and equal to Is

This constancy is the reason behind the hame saturation current.

$$r_d = \frac{\gamma V_T}{\hat{i}_b + I_s} \approx \sum_{i_b \approx -I_s}^{\infty} \frac{\text{Reverse dynamic}^n}{\text{resistance}}$$

The breakdown region is entered when the magnitude of the reverse voltage exceed a threshold value called the breakdown voltage or the zener knee voltage.

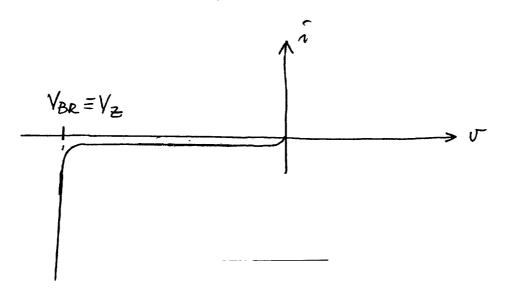
In the breakdown region the reverse current increases rapidly with a very small increase in the associated voltage.

The breakdown voltage is sometime collect the peak inverse voltage (PIV) in manufacturer's specification sheets.

At breakdown there is an avadanche of electrons which flow across the junction with the result that the diode over heats.

The large current can destroy part of the diode (the portion that overheats).

Provided that the power dissipated in the diode is limited by external circuitry to a safe level (usually provided on the data sheets) breakdown Won't be destructive.



TEMPERATURE EFFECTS

The diode characteristic has 2 terms, Vy and Is Which are heavily dependent on temperature.

$$V_T = \frac{kT}{9} = \frac{T}{11600}$$

$$\frac{I_S}{A} = 9m_t^2 \left(\frac{D_P}{N_D L_P} + \frac{D_D}{N_A L_D}\right) \sim V_T \text{ through Etnstein relation}$$

For silicon Is increase approximately 15% per °C (Ki = 0.15/°C) or in other terms Is doubles every 5°C

$$T_s(e\tau_2) = T_s(e\tau_i)/5$$

$$I_s(@T_2) = I_s(@T_i)e^{ki(T_2-T_i)} = I_s(@T_i)e^{(T_2-T_i)/7}$$

I have a value and I want it to become 1.15 times bigger every time I add a oc

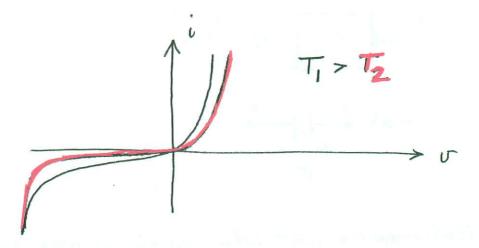
I need some mechanism that transform an addition in a multiplication

$$-\frac{b^{x+y}}{b} = b^{x} \cdot b^{y}$$

$$b^{0.15 \cdot 1} = 1.15$$

$$b^{0.15 \cdot 2} = b^{0.15(1+1)} = b^{0.15}, b^{0.15} = 1.15 \cdot 1.15$$

As T increases in order to mantain a constant value of I voltage must be reduced. For silicon $\frac{dV}{dT} \simeq -2.0 \text{ mV/C}$

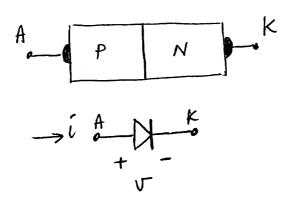


$$2^{\times} = 1.015 \implies \log_{2} 1.015 = \times$$

$$\log_{2} y = \frac{\ln y}{\ln 2} = \frac{\log_{10} y}{\log_{2} 2}$$

$$\log_{2} 1.05 = \frac{\ln 1.05}{\ln 2} = \frac{1}{5}$$

Semiconductor diodes are formed by a projunction



The semiconductor materials commonly used are; germanium, silicon, and gallium arsenide, (GaAs is particularly used in microwave applications, photo-detection and laser diodes)

The unbiased p-n junction

₽		N
+++++ +++++ +++++ +++++	0000	(H) (1) (1) (1) (1) (1) (1) (1) (1) (1) (1

+ majority holes

- majority free electrons

In the p-type material for simplicity are not shown the negative charges (in equal amount to the hous) associated with the aonized acceptor atoms and the minority precedectrons generated by thermal agitation.

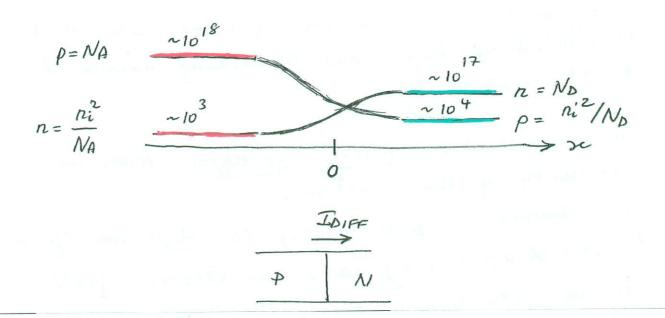
Similarly in the n-type material are not shown the positive charges associated with the ionized donor atoms and the minority holes generated by thermal agitation.

DIFFUSION CURRENT

Because the concentration of holes is high in the p-region and low in the n-region, holes diffuse across the junction from the p side to the n side

Similarly the electrons diffuse across the junction from the n side to the p side

These two components add together to form a diffusion current IDIFF whose direction is from the p side to the p side



The holes that diffuse across the junction into the n region will meet a high concentration of electrons so they quickly recombine disappearing from the scene.

The electrons that diffuse across the junction into the pregion will quickly recombine with some of numerous holes present on the pside, thus disappear from the scene.

J

As result there will be: a region close to the junction (on the p side) that is depleted of free electrons and contains uncovered bound positive charge and

a region close to the junction (on the p side) that is depleted of holes and containing uncovered bound regative charge

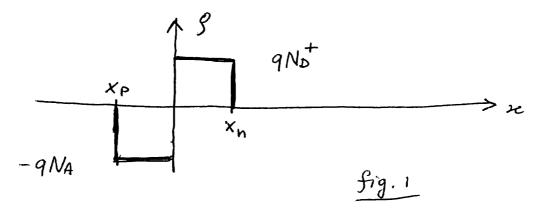
it follow that a space-charge region forms in proximity of the junction.

The charges on both side of the depletion region (= space charge region) course an electric field to be established across the region.

(hence a potential difference result across the region with a side at positive voltage relative to the p side)

The resulting electric field apposes the diffusion of holes into the n region and electrons in the p region

The voltage drop across the depletion region acts as a <u>barrier</u> that has to be overcome for holes to diffuse into the n region and electrons to diffuse into the p region.



Gauss' Law :

$$\frac{dE_n}{dx} = \frac{g}{E_{si}}$$

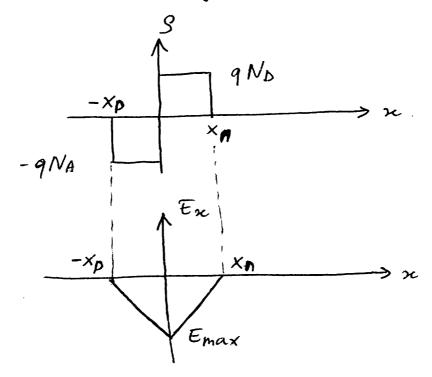
$$S = 9 \left(\rho - n + N_D - N_A \right)$$

The depletion region
is free of electrons and holes $N_{D}-N_{A} >> \rho-n$

1 on the p side No-0

$$\frac{dEx}{dx} = -\frac{9NA}{E_{si}}$$

$$\frac{d\mathcal{E}_n}{dn} = \frac{9ND}{\mathcal{E}_{si}}$$



$$\frac{\mathcal{E}_{x}(n)}{\int d\mathcal{E}_{x}} = -\frac{9NA}{\mathcal{E}_{si}} \int_{-\mathbf{X}p}^{x} dn$$

$$E_{x}(x) - E_{x}(-x_{p}) = \frac{-qN_{A}}{E_{s}}(x + x_{p})$$

boundary of the space charge region

$$\frac{E_{x}(x) = -\frac{qNA}{E_{si}}(n + np)$$

$$E_{x}(o) = E_{max} = -\frac{9N_{A}}{E_{si}} \times p$$

$$\frac{E(x_n)}{\int dE_x} = \frac{qN_0}{\mathcal{E}_{s_i}} \int_{x} dx$$

$$\underbrace{\mathcal{E}(n_{\mathbf{n}})}_{n} - \underbrace{\mathcal{E}(n)}_{n} = \frac{qN_{b}}{\mathcal{E}_{si}} (x_{\mathbf{n}} - x)$$

$$E_{\kappa}(\kappa) = \frac{-9N_{\rm b}}{E_{\rm ci}} \left(\chi - \chi\right)$$

$$E_n(o) = E_{max} = -\frac{9N_0}{E_{Si}} \times n$$

Thus:

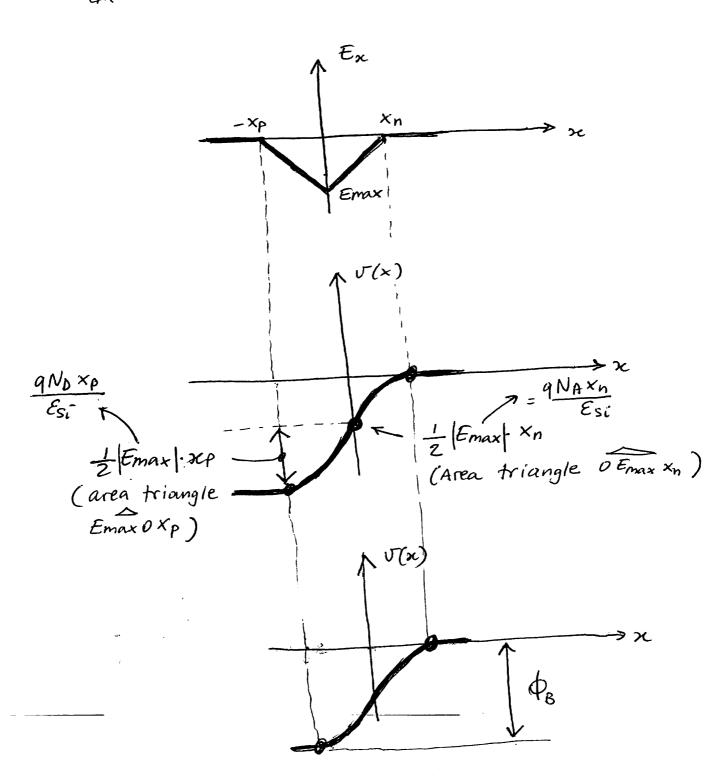
$$E_{x}(o) = E_{max} = \frac{-9No}{E_{si}} \times_{n} = \frac{-9NA}{E_{si}} \times_{p}$$
Field at the junction



The width of the depletion region will not be the same on the 2 sides.

Recalling how potential and electric field are related

$$\frac{dv}{dx} = -E(x) \longrightarrow dv = -E(x)dx$$



$$\phi_B = \text{ junction built-in voltage} =$$

$$= \frac{1}{2} 9 \frac{N_b}{\mathcal{E}_{si}} \times \mathbf{n}^2 + \frac{1}{2} \frac{9N_A}{\mathcal{E}_{si}} \times \mathbf{p}^2$$

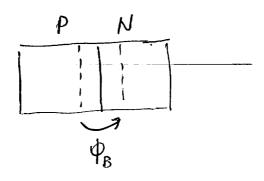
Recalling that:

$$N_{D} \times_{\mathbf{n}} = N_{A} \times_{\mathbf{p}} \implies \begin{cases} \times_{\mathbf{p}} = (N_{D}/N_{A}) \times_{\mathbf{n}} \\ \times_{\mathbf{n}} = \frac{N_{A}}{N_{D}} \times_{\mathbf{p}} \end{cases}$$

$$X_{dep} = \times_{\mathbf{p}} + \times_{\mathbf{n}} = (\frac{N_{A}}{N_{D}} + 1) \times_{\mathbf{p}} = (\frac{N_{D}}{N_{A}} + 1) \times_{\mathbf{n}} \end{cases}$$

$$X_{\mathbf{p}} = X_{dep} \frac{N_{D}}{N_{D} + N_{A}}$$

$$X_{\mathbf{n}} = X_{dep} \frac{N_{A}}{N_{A} + N_{A}}$$



As already noticed since usually the deping levels are not equal in the p and n materials The width of the depletion region will not be the same on the two sides

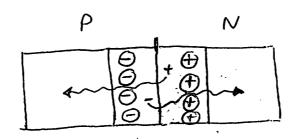
-) in order to uncover the same amount of charge the depletion layer will extend deeper into the

more lightly deped material. ACCEPTORS

Equilibrium

Across the junction: In addition to the current component IDIFF due To the majority carrier diffusion there is as well a component due to minority carrier (15).

Specifically some of the thermally generated holes in the n material travel through the I material to the edge of the depletion region. There they experience the electric field in the depletion region, which , them across that region into the p side.



Similarly some of the thermally generated free electrons in the p material reach the edge of the depletion region and get swept by the electric field in the depution region across that region into the n-side.

These two 1 components electrons moved by drift from p to N and holes moved by drift from N To P add together to form a drift current Is, whose direction is from the N side to the P side

Under the open-circuit condition no current exists thus the two apposite currents across the Junction must be equal

J = Jp = Jn = 0

$$E_{x} = -\frac{dv}{dx}$$

$$\int_{0}^{\pi} \int_{0}^{\pi} \int_{0$$

$$J_n = q \mu_n n \, \mathcal{E}_{\mathcal{X}} + q \, \mathcal{D}_{\mathcal{P}} \, \frac{dn}{dx} = 0 \quad (2)$$

$$p(x) = p(x') e^{-\frac{\sigma(x) - \sigma(x')}{\kappa \tau / 9}}$$

$$n(x) = n(x') e^{\frac{\sigma(x) - \sigma(x')}{KT/9}}$$

solution of the differential eq. (2) is:

SEE HAMDOUT #7



$$P(\infty) = P(-\infty) e^{-\frac{\Phi_B}{\kappa T/q}}$$

$$n(\infty) = n(-\infty) e^{\frac{\Phi_B}{\kappa T/q}} (*)$$

$$\begin{array}{c|c}
P & N \\
\hline
-\infty & +\infty
\end{array}$$

$$\rho(-\infty) \approx N_A$$

$$h(-\infty) = \frac{n_i^2}{N_A}$$

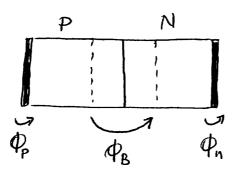
$$n(+\infty) \cong N_D$$

$$p(+\infty) = \frac{n_i^2}{N_D}$$

$$N_{D} = \frac{n_{i}^{2}}{N_{A}} e^{\frac{\Phi_{B}}{KT/Q}} - D \frac{N_{D}N_{A}}{n_{i}^{2}} = e^{\frac{\Phi_{B}}{KT/Q}}$$

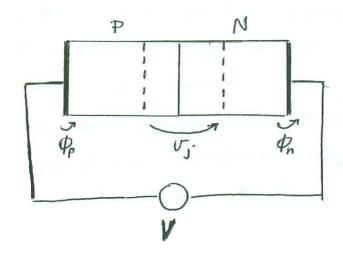
Typically for silicon at room temperature ϕ_B is in the range $0.6 \div 0.8 \text{ V}$ $\Rightarrow 26 \text{ mV. ln} \frac{10^{18} \cdot 10^{17}}{10^{21}} \approx 0.83$ NOTE ϕ_B is not V_Y !!!

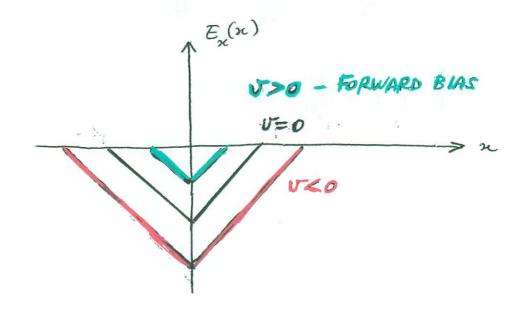
When the p-n junction terminals are left open-circuited the voltage measured between them will be zero! That means that the voltage of across the depletion region does not appear between the diode terminals. This is becomes of the contact voltages existing at the metal-semiconductor junctions at the drode terminals. That counter-balance the barrier voltage.



$$\phi_p + \phi_p + \phi_n = 0$$

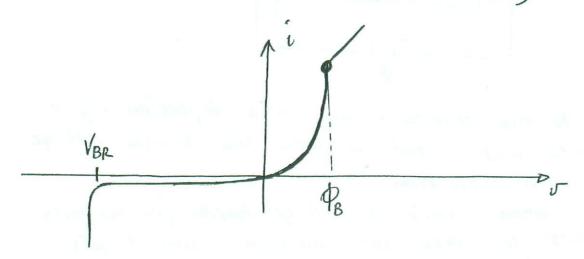
The BIASED P-N Junction





If I keep decreasing the voltage too much eventually I'll reach a breakdown situation (depletion region can't get brigger than the length of the semiconductor bar !!!)

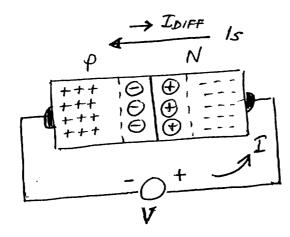
If I keep increasing the voltage eventually the depletion region will disappear (when $v=\phi_8$) As v becomes comparable with ϕ_8 the ϕ_8 junction behaves like a soit of resistor (the current is governed by the ohmic-contact and the semiconductor-bulk resistance)



$$\phi_{\rm B} = \frac{KT}{9} \ln \frac{N_{\rm A}N_{\rm D}}{n_i^2}$$

$$E_{max} = \sqrt{\frac{zq}{\mathcal{E}_{S_c}}} \frac{N_A N_D}{N_{A+N_D}} (\phi_B - \sigma)$$

$$\times_{\text{dep}} = \sqrt{\frac{2 \mathcal{E}_{si}}{9} \frac{N_A + N_D}{N_A N_D} \left(\phi_B - \sigma \right)}$$



Due to the reverse voltage the depletion region becomes wider, and so does the barrier voltage across the junction. This means that it will get harder for majority carriers to cross the junction, but it gets easier for the minority carriers to be swept (drifted) from one side to the other.

$$I = I_s - I_D \approx I_s$$

To dominates I_{DIFF}

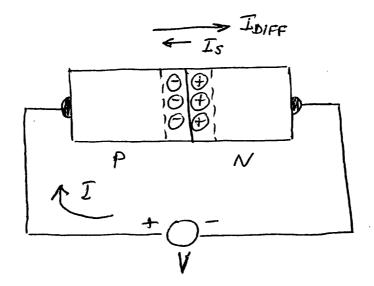
If we keep decreasing the voltage the depletion region becomes wider and wider until at a certain point there is a new phenomenon that will set in and supply the charge carriers! This is called breakdown!!

There are two mechanism that contributes to the breakdown:

- * zener effect
- * avalanche effect
- → If |VBR > 5V usually the breakdown is due to Zener effect.
- -DIF |VBR |> 7V usually the breakdown is due to avalanche effect.
- -o For junctions that breaks down between 5 and 7 V usually we have a combination of the two.

ZENER BREAKBOWN -D occurs when the electric field in the depletion layer is strong enough to break covalent bonds and generate electron-hole pairs

AVALANCHE BREAKDOWN - The minority carriers that cross the junction under the influence of the electric field gain enough kinetic energy to be able to break covalent bonds in atoms with which they collide.



Due To the forward voltage the depletion region shrink, and so does the voltage barrier across the junction. This means that it will be easier for the majority carriers to overcome the barrier and therefore cross the junction but it is tougher for the minority carriers to be drifted all the way from one side to the other.

Current - voltage relationship

$$J = \frac{J}{A} \rightarrow J = A \cdot J$$

There are two contributes: one due to the minority carriers and the other due to the majority carriers.

The contribute due to the majority carriers is the diffusion current the contribute due to the minority carrier is the drift current

It can be shown that:

$$J = \left(\frac{q D_{p} n_{i}^{2}}{4 p N_{D}} + \frac{q D_{n} n_{i}^{2}}{4 n N_{A}}\right) \left(e^{V/V_{T}} - 1\right)$$

$$\frac{n_i^2}{N_D}$$
 = concentration of holes in the N region (\rightarrow minory carriers)

$$\frac{n_i^2}{NA}$$
 = concentration of the electrons in the P region (-) minority carriers)

De diffusion constant for holes in the N-type silicon

Lp diffusion length of holes in the N-type silicon

To average time it takes for a hole to into the n-type silicon to recombine with a majority electron

$$I = A \cdot J = Aqn_i^2 \left(\frac{D_P}{L_P N_D} + \frac{D_n}{L_n N_A} \right) \left(e^{V/V_T} - 1 \right)$$

$$I_S$$

DIODE CAPACITANCES

Depletion capacitance

The depletion layer stores a charge of equal amount on each side of the junction. - D it forms a capacitance !!

$$q_{j} = q_{N} = qN_{D}x_{n}A = q_{p} = qN_{A}x_{p}A$$

$$q_{j} = q \frac{N_{A}N_{D}}{N_{A}+N_{D}}Ax_{dep}$$

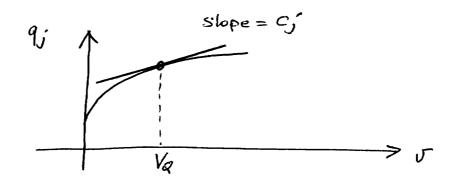
and recalling what we found some time ago:

Xdep =
$$\sqrt{\frac{2 \mathcal{E}_{si}}{9}} \frac{N_A + N_D}{N_A + N_D} (\phi_B + v)$$

9j-5 relationship is not linear!! so this is a non linear capacitor!!

$$q_j \propto \sqrt{\sigma}$$

Obviously a linear-copacitance approximation can be done if the device is biased and signal swing around the bias point is small!



$$C_j = \frac{dg_j}{dv} \bigg|_{v=V_Q}$$

or using the familiar parallel-plate capacitor formula:

$$C_{j} = \frac{\mathcal{E}_{S} \cdot A}{\chi_{dep}} = \frac{\mathcal{E}_{S} \cdot A}{\sqrt{\frac{z \mathcal{E}_{S}}{q} \cdot \frac{NAtN_{D}}{N_{A} \cdot N_{D}}} (\phi_{B} - J)} =$$

$$= \frac{A}{\sqrt{\frac{2}{9E_S} \left(\frac{NAtN_D}{NA\bullet N_D}\right) \left(\phi_B - \sigma\right)}}$$

$$= \frac{A}{\sqrt{\frac{2}{9 \, \mathcal{E}_{S}} \left(\frac{NA+N_{D}}{N_{A} \cdot N_{B}}\right) \left(\frac{\varphi_{B} - \sigma}{\varphi_{B}}\right) \frac{\varphi_{B}}{\varphi_{B}}}}$$

$$= \frac{2}{\sqrt{\frac{2}{9E_{S}}\left(\frac{NAtN_{D}}{N_{A} \cdot N_{D}}\right)\left(1 - \frac{U}{\phi_{B}}\right)\phi_{B}}}$$

$$C_{jo} \triangleq \frac{A}{\sqrt{\frac{2}{9E_{s}} \left(\frac{NAtN_{D}}{NA \cdot N_{D}}\right) \phi_{B}}}$$

Therefore we can write

$$C_{j} = \frac{C_{jo}}{\sqrt{1 - \frac{v}{\varphi_{B}}}}$$

The analysis is based on the assumption that the carrier concentration change absuptly at the junction boundary.

More in general

$$C_{j} = \frac{C_{jo}}{\left(1 - \frac{\sigma}{\phi_{B}}\right)^{m_{j}}}$$

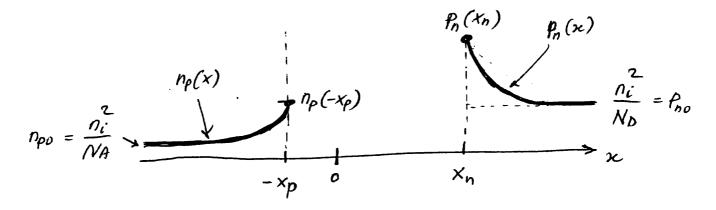
where mj is called GRADING COEFFICIENT and its value ranges from \$ to \$\frac{1}{2}\$ depending on the manner in which the concentration changes from the \$P\$ to \$N\$ side of the junction.

Diffusion Capacitance

in the vicinity of the junction on the N side we have greater hole concentration than normally exists (-> because of diffusion).

This excess hole density can be considered as charge storage in the neighborhood of the junction.

Similar statement apply to electrons which diffuse into the p region



The excess hole charge stored in the n region is given by:

$$Q_{p} = A \cdot q \cdot \left[P_{n}(x_{n}) - P_{no} \right] \cdot L_{p} = \frac{1}{P_{n}(x_{n})} = \frac{1}{P_{no}(x_{n})} = \frac{1}{P_{no}$$

$$Q_n = I_n \cdot Z_n$$

The total excess minority-carrier charge is:

since the drode current $I = I_p + I_n$ we can express the excess charge as:

where c_T is called diode mean transit time. Pratically since usually $N_A >> N_B \rightarrow I_P >> I_n$ then $I \approx I_P$ and $Q_P >> Q_R \rightarrow P$ $Q \approx Q_P$ and thus $c_T \approx c_P$ This solve the problem of finding out c_T !

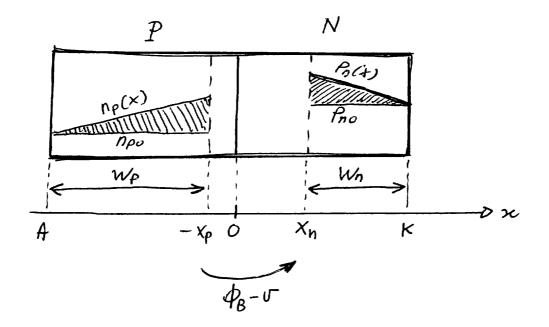
For small changes around a bias point:

$$C_0 = \frac{dQ}{dV} \Big|_{V=V_Q}$$

$$C_{D} = \frac{d(2\tau I)}{dV} = \frac{\tau_{\tau}(\frac{dI}{dV})}{|V|} = \frac{1}{V_{z}}$$

and we found some time ago that:

$$g_{diode} = \frac{I_{pione} + I_{s}}{V_{T}}$$



There is electric field only in the space-charge region (between -xp and xn)

Therefore the region from A to -xp and from In to K are quasi neutral !!

The boundary of the quasi-neutral p-region is at -xp and the hole density there must be equal at equilibrium as well as under bias

The same is true for the electron density at the boundary of the quasi-neutral n-region at xn

at
$$x_n$$

$$\int \frac{can be shown}{(see Muller-kamins p. 234)}$$

$$\frac{n_p(-x_p) = n_{po} e}{p_n(x_n) = p_{no} e}$$

The current that flows through any transverse section x must be constant and has the contribute of both holes and electrons:

If we consider the quasi-neutral regions than since there is no freld in those regions there will be no drift:

$$I_n \approx I_n$$
, diff (in the neutral region W_n)
 $I_P \propto I_P$, diff (in the neutral region W_P)

On this basis, the most suitable transverse sections for the evaluation of the total current I DIODE are those at the boundary of the depletion layer -> x=-xp or x=xn

$$\overline{I}_{DIODE} = \overline{I}_{n}(-x_{p}) + \overline{I}_{p}(-x_{p})$$

since the flux of the carriers is constant in the depletion layer (-> simplifying assumption !!)

$$I_{\rho}(-x_{\rho}) = I_{\rho}(x_{n})$$

$$\overline{J}_{DLODE} = \overline{I}_{n}(-x_{p}) + \overline{I}_{p}(x_{n})$$

currents of the minority corriers

The diffusion currents are a to the gradient of the distribution of the carriers:

(2)
$$I_{P,diff}(x) = -qAD_{P}\frac{dP_{n}(x)}{dx}$$
 (for holes)

I assume linear distributions!!

$$\frac{dnp}{dx} = \frac{n_p(-x_p) - n_p(A)}{Wp} = \frac{n_{po}e - n_{po}}{Wp}$$
SHORT
$$\frac{dnp}{dx} = \frac{n_p(-x_p) - n_p(A)}{Wp} = \frac{v/v_p}{V/v_p}$$

$$\frac{dP_n}{dx} = \frac{-P_n(x_n) + P_n(x)}{W_n} = \frac{-P_{no}e^{V/V_T} + P_{no}}{W_p}$$

$$\frac{dnp}{dx} = \frac{n_{i}^{2}}{N_{A} \cdot W_{p}} \left(e^{-1} \right)$$

$$n_{po} = \frac{n_{i}^{2}}{N_{A}} \left(e^{-1} \right)$$

$$\frac{dP_n}{dx} = \frac{-n_u^2}{N_b \cdot W_n} \left(e^{\sqrt{V_T}} \right)$$

$$P_{no} = n_i^2 / N_b$$

Substituting in 1 and 2

$$O ln,diff(Xp) = \frac{n_i^2}{N_A W_P} q_A D_n \left(e^{-1}\right)$$

$$(2) I_{P, diff}(x_n) = \frac{n_i^2}{N_D W_n} q A D_P (e^{-1})$$

$$\overline{J}_{DIOBE} = \frac{qAn_i^2}{\sqrt{N_A W_P}} \left(\frac{D_n}{N_A W_P} + \frac{D_P}{N_D W_n} \right) \left(e^{-1} \right) \\
\overline{J}_S$$

In the case of a LONG DIODE:

$$\mathcal{J}_{DOSE} = 9An_c^2 \left(\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p}\right) \left(e^{\sigma/V_T}\right)$$

$$\mathcal{J}_{S}$$

A the minority carriers will recombine before reaching the drode terminals !!!

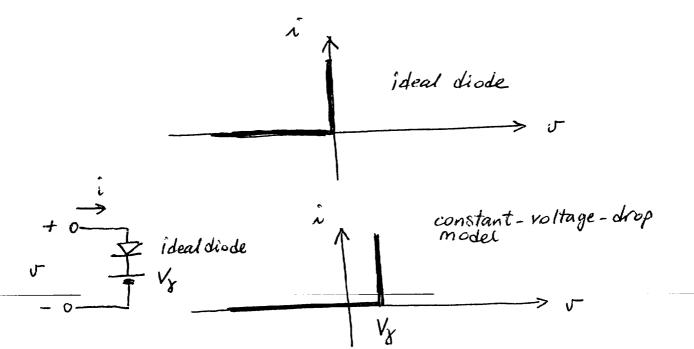
If one is doing a pencil and paper design of a relatively complex arount, rapid arount analysis is a necessity

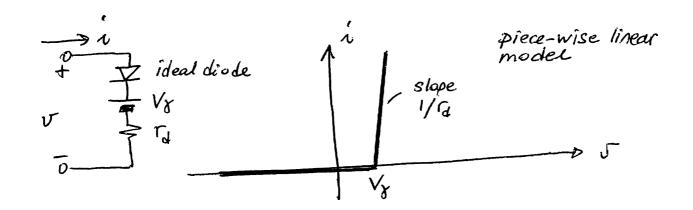
we want to quickly evaluate various possibilities before committing to a suitable circuit topology. More accurate analysis can be postponed until the almost final design is obtained -> possibly with the aid of a computer circuit-analysis program (e.g. SPICE), then

The accurate can be used to further refine (fine-tune) the design.

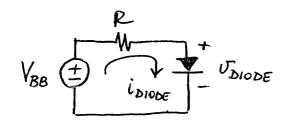
The issue is of finding an appropriate compromise between accuracy and complexity.

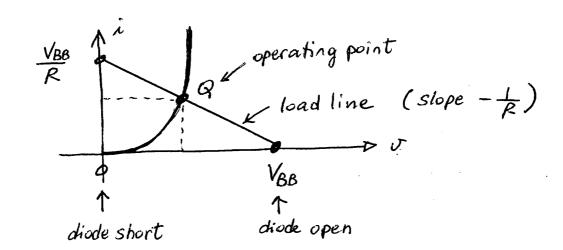
Different simplified models of the diade are commonly used.





The Load Line concept



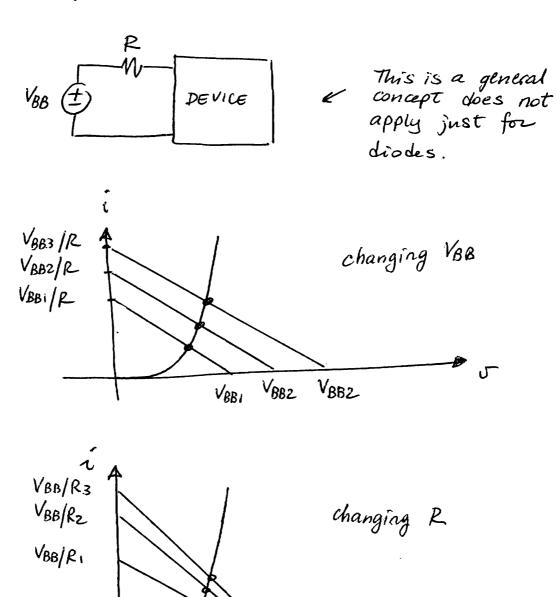


$$V_{BB} = Ri_{DIODE} + U_{DIODE} - D i_{DIODE} = \frac{V_{BB}}{R} - \frac{V_{DIODE}}{R}$$

this is the equation of a line:

y = a - bx

The intersection of the load line with volt-ampere carachteristic of the diode gives the operating values of voltage and current in the circuit.



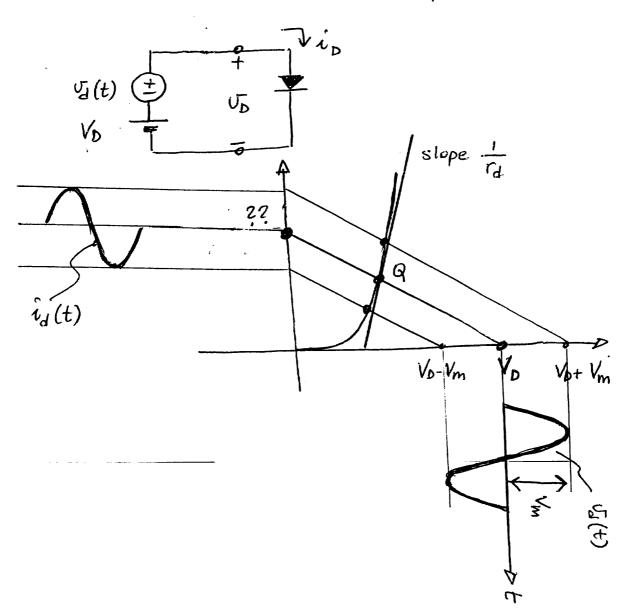
 V_{BB}

Small signal model

So far we have been mainly focused on using the ON-OFF behavior of the diode. In these applications usually the applied signal is relatively large so the models seen so far are more than adequate!

1

There are other application where the diode is biased to operate at a certain point (Vox, IDA) on the i-v characteristic and a small ac signal is superimposed on the dc quantities



5.22 When the signal of (t) is absent the diode voltage is equal to

and the diode will conduct a dc current

when the signal of (t) is applied the total istantaneous diode voltage will be given by

correspondingly the Total istantaneous current îs(t) will be:

$$I_D(t) \cong I_S e$$

$$= (V_D/\eta V_T) I_S/\eta V_T$$

$$= I_S e e =$$

$$f(x) = f(x_0) + f'(x_0)(x-x_0) + \frac{f'(x_0)(x-x_0)^2}{2!} + \dots$$

TAYLOR EXPANSION

$$ax = ax_0 = ax_0$$

$$e = e + ae (x-x_0) + \dots = A$$

$$= 1 + ax + \dots$$

$$x_0 = 0$$

Therefore if
$$\frac{U_d}{\eta V_T} \approx 0$$
 (as rule of thum b take amphitudes smaller than 10 mV)

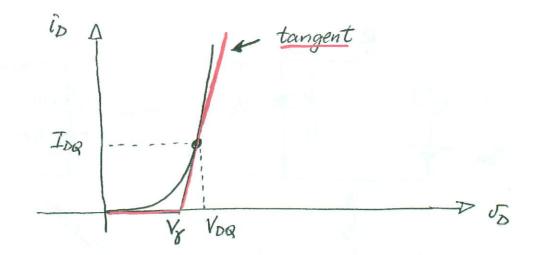
 $i_D(t) \cong I_{DQ} \cdot \left(1 + \frac{U_d}{\eta V_T}\right) - D$

$$i_d(t) = \frac{I_{DQ}}{\gamma V_T} J_d(t)$$

$$\frac{\eta V_T}{I_{DR}} \triangleq \pi_d$$
 diode small signal resistance incremental resistance

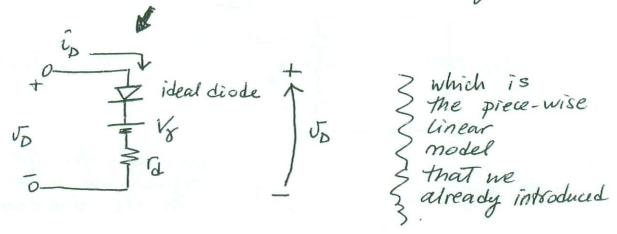
FORWARD BIASED DIODE !!!

If we look at what we have done from a graphical perspective;



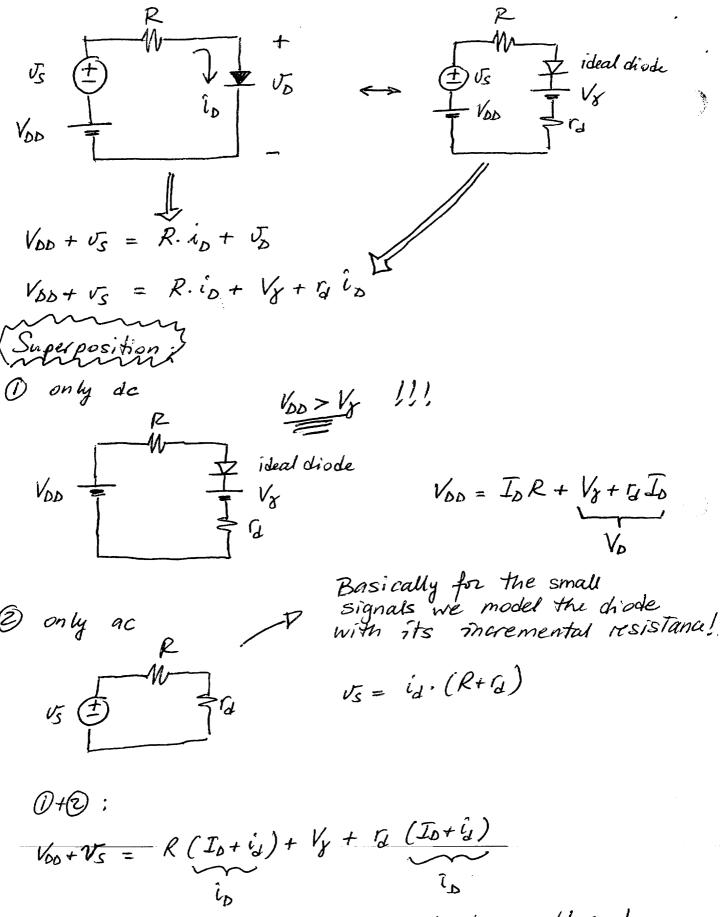
$$\hat{l}_D = \frac{1}{r_d} (v_D - V_g)$$
 = equation of the tangent to the i-v diode curve at (V_{DQ}, I_{DQ})

For small signals we can reasonably approximate the diode i-or curve with its tangent:



The circuit we have analyzed is soit of problematic when we want to set IDA !!!

Pratically that's what we do:



So this approach where we separated dc world and ac world (for small signals) makes sense !!!

So far we have totally neglected the diade charge storage effects.

This is reasonable only when the small signals we apply have a frequency that is relatively small

If the frequency goes up we have to account for Cj and Cd

 $\begin{array}{c|c}
c_1 & c_2 \\
\hline
c_4 & c_4
\end{array}$

For Low frequencies

C; and Cd are open circuits

but for high frequencies

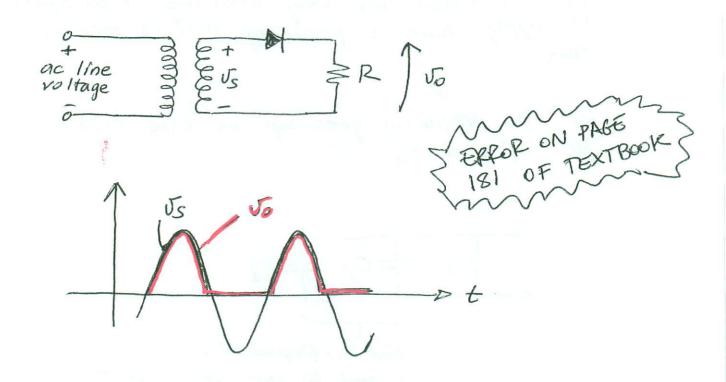
C; and Cd becomes short arcuits !!

It takes time to switch the diode ON-OFF and viceversa !!

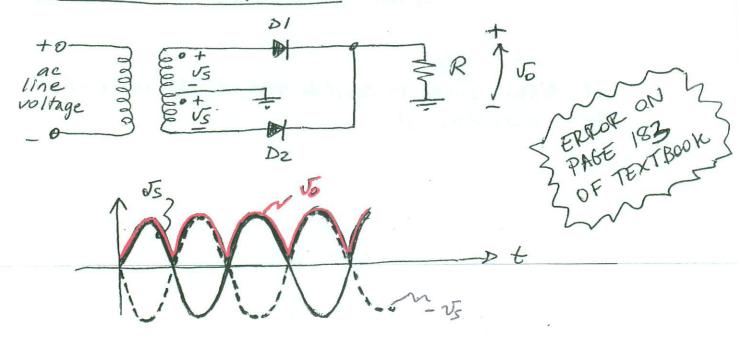
Elementary diode applications

· Rectifiers

Half wave rectification



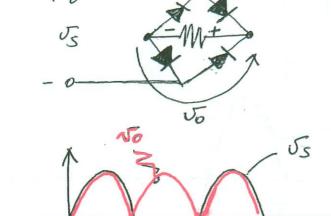
Full-wave Rectification

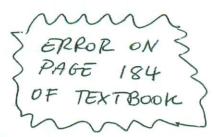


PIV of the diodes is about 21/s !!!
peak inverse voltage

bridge rectifier

(Gratz)

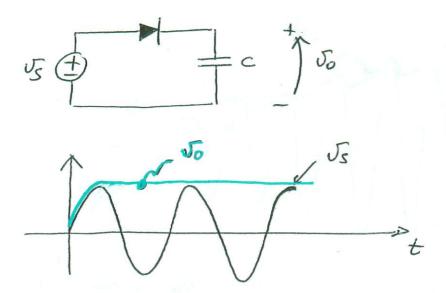


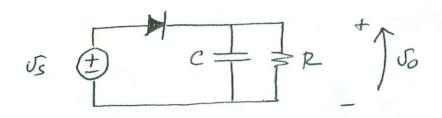


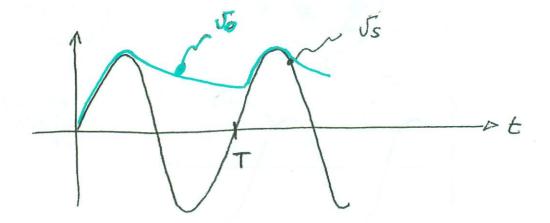
PIV of the diodes is about Vs !!

Peak Rectifier - (Rectifier with capacitive filter)

peak detector (can be used to reconstruct the envelope of an AM signal)

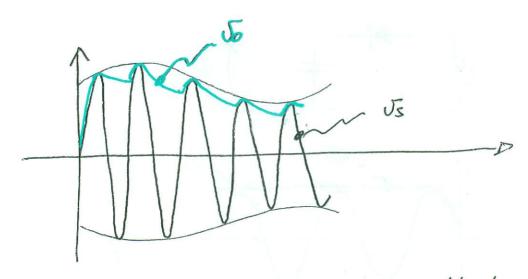




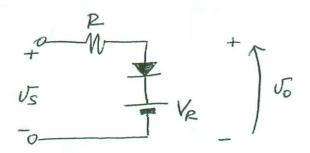


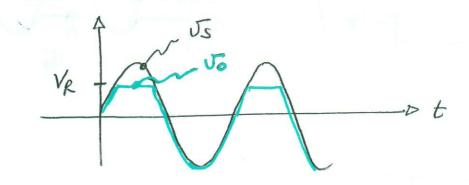
we have to choose >> T

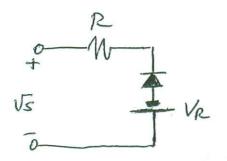
during the discharge -> Vo = Vp e

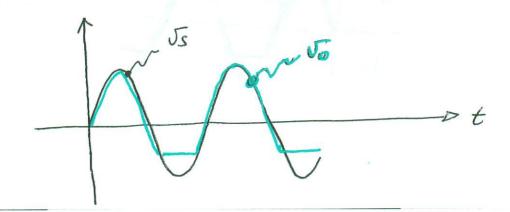


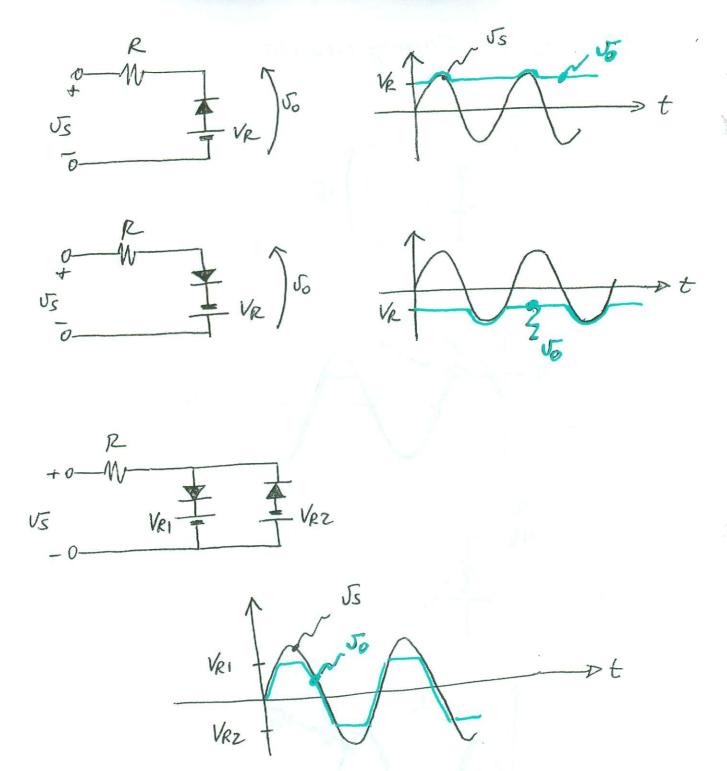
If I feed an AM signal to this circuit it will detect its envelope





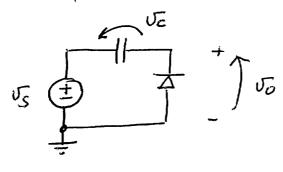


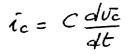




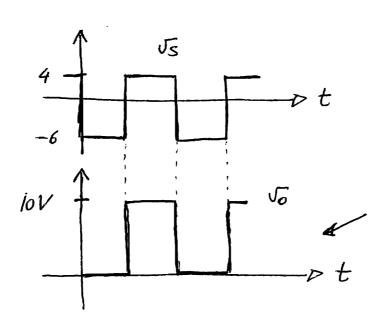
CLAMPING CIRCUITS

Clamping is a shifting operation of a waveform, where the amount of shift depends upon the actual waveform.



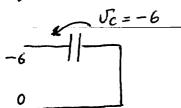


This is a though circuit to analyze



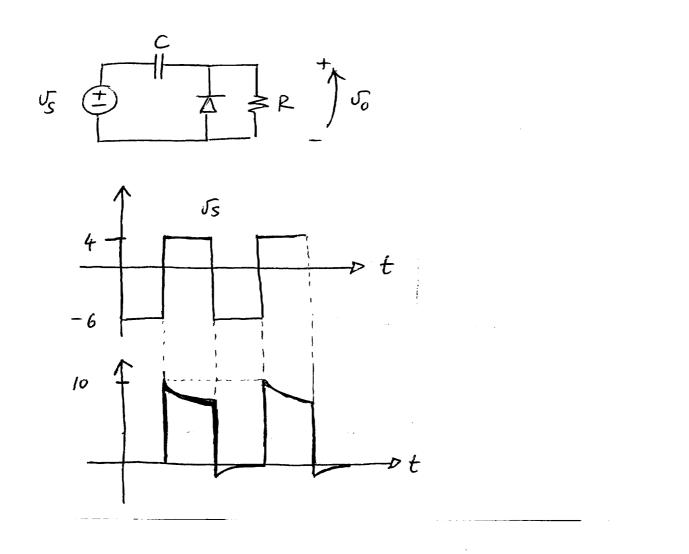
DC RESTORATION!

At the beginning the diode is a short and the capacitance will charge to a voltage \sqrt{c} equal to the magnitude of the most negative peak $(\sqrt{c} = -6\sqrt{c})$

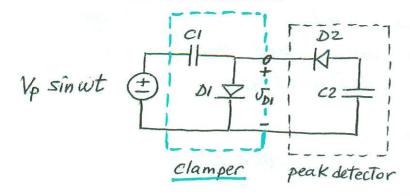


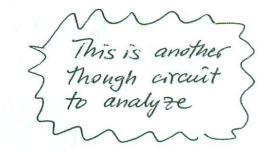
Subsequently the diode open and the capacitor retains its voltage indefinitely.

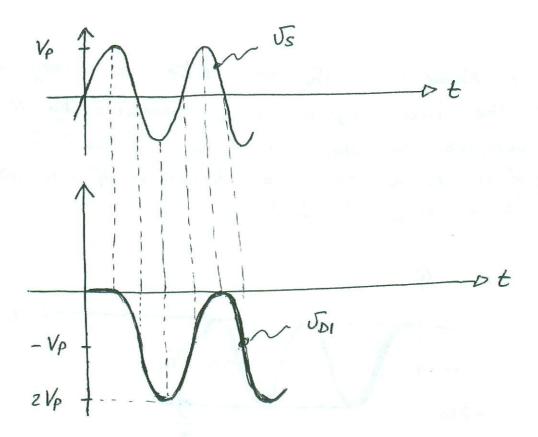
More pratically there will be a load resistance connected across the diode in a damping circuit



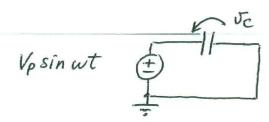
VOLTAGE DOUBLER



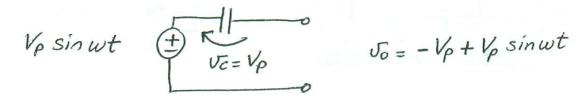




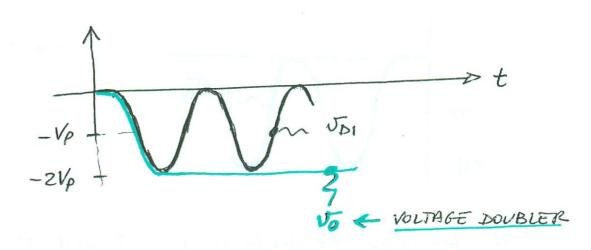
at the beginning the diode is a short and the capacitance will charge to a voltage ve equal to Vp.



Subsequently after $\frac{\pi}{2}$ when the sine wave has reached is peak value and CI is now charged at $v_c = v_p$ the diode open and the copacitor retains its voltage indefinitely



once we know how JD, looks like it's very easy to get the final output voltage produced by the peak detector (> note that here I want to detect a negative peak so the direction of the diode DZ must be properly set !!)

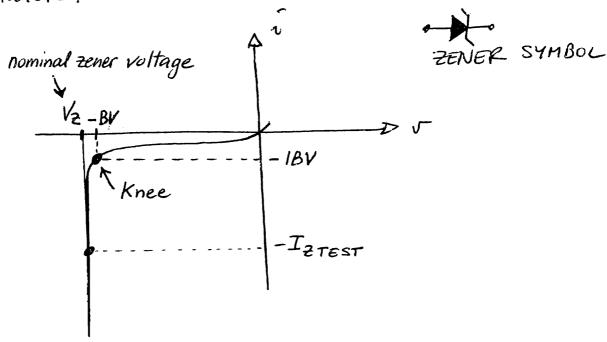


A zener diode is a device where the doping is performed in such a way as to make the i-v-characteristic in breakdown region very steep.

If the reverse voltage exceeds the breakdown voltage the diode normally will not be destroyed.

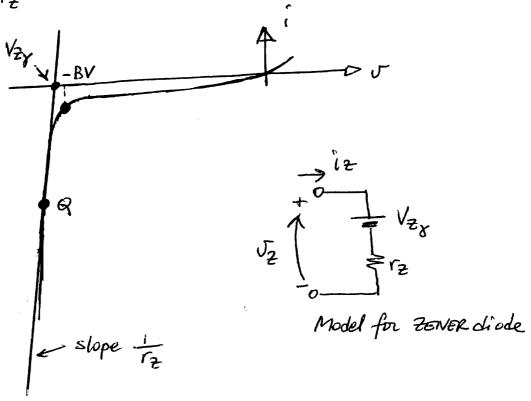
(the mannfacturer specifies the maximum power that the device can safely dissipate - P sometimes they give directly the max current that the device can safely tolerate)

the almost constant voltage drop that the diade exhibits in the breakdown region suggest that a natural application could be in the design of voltage tegulators.



The manufacturer usually specifies the "nominal" voltage across the zener Vz at a specified test current Izrest.

Though the i-v curve is very steep in the breakdown region it is not vertical — it has a certain slope — 1

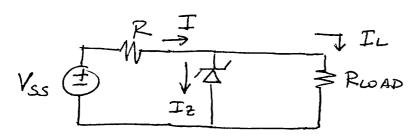


pratically it is often assumed that $V_{ZX} \approx -BV$ there voltage

The maximum reverse current Izmax that the zener can withstand is dependent upon the design and construction of the diode.

The leakage current (Izmin) at the knee of the caracteristic curve is sometime assumed 10% of the IImax (>) Izmin is what we also colled IBV)

in lack of more accurate data !!!



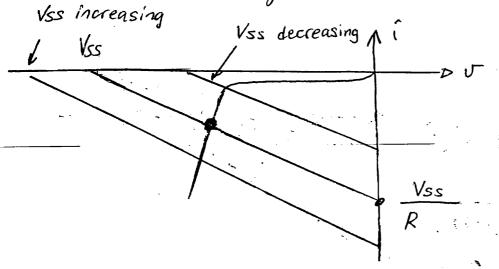
It's given a supply rollage knominally 10V but that can kary by ± 1V.

We want to design a voltage regulator able to provide a constant voltage of 6.8 V to a load RL. The load can vary from 0.5 KSZ to 2KSZ.

We have a Zener specified to have $V_Z=6.8$ at $I_Z=20\,\text{mA}$. I_Z is about 5 sr and the max current that the zener can with stand is about 60 mA (ZENER IN754)

1

In order to properly design this circuit the resistance R must be such that the diode stays in the constant voltage region over the entire range of input voltages and load impedance!!



$$V_{SS} = \begin{array}{c|c} P & \overline{J} \\ \hline V_{SS} & \overline{J} \\ \hline \end{array}$$

$$\begin{cases}
V_{SS} - V_{Z} = R \cdot I \\
I = I_{Z} + I_{L} \longrightarrow I = I_{Z} + \frac{V_{Z}}{R_{L}}
\end{cases}$$

In order to assure that the diode remains in the constant voltage region, there are two extreme conditions to consider:

The highest current through the diode occurs when the source voltage is maximum and RL is maximum (-> the worst thing that can happen is that the load get unconnected because then all current supplied I goes through the diode)

$$I_{2max} = \frac{V_{smax} - V_{2}}{R} I_{lmin} = \frac{V_{ssmax} - V_{2}}{R}$$

$$= \frac{V_{ssmax} - V_{2}}{R} \frac{V_{2}}{R_{lmax}} \frac{1}{R_{l\rightarrow\infty}}$$

$$= \frac{V_{ssmax} - V_{2}}{R}$$

The lowest current through the diode occurs when the source voltage is minimum and RL is minimum (-> most of current supplied I is drawn by RL)

$$I_{2min} = \frac{Vss_{min} - V_2}{R} - I_{L_{max}} = \frac{Vss_{min} - V_2}{R} - \frac{V_2}{R_{Lmin}}$$

Let's try now to select R based on the nominal values (-> intermediate case) but assuming that there is no load (-> all current provided by the power supply will flow through the zener -> we are over-pessimistic -> just to be be on the safe side)

$$I_{Znom} = \frac{V_{SS} - V_{Znom}}{R} - D R = \frac{V_{SS} - V_{Znom}}{I_{Dom}}$$

Let's now verify if this choice of R will satisfy the 2 extreme situations!!

$$I_{t_{max}} \leq \frac{V_{ss_{max}} - V_{t}}{R} \approx 27 \text{ mA}$$

The sener can stand up to 60 mA so that's fine !

$$= \frac{9-6.8}{160} - \frac{6.8}{500} \approx 0.2 \text{ mA}$$

HERE WE have a problem !!

The current at the knee is about 6mA (-> 10% of 60 mA) so we are not in the constant voltage

we need to lower R!

In order to remain in the constant voltage region we need to choose R in such a way that:

$$R \leq \frac{Vssmin - Vz}{I_{2min} + I_{L_{max}}} = \frac{9 - 6.8}{6 \times 10^{-3} + \frac{6.8}{500}}$$

I need more current, so more current Will flow through the tener

~ 112 SV

Let's than take R=100-52 and cross-check what happen:

In order to evaluate how good the voltage regulator we designed we imeasure the total voltage swing divided the nominal voltage (provided to the load)

PERCENT =
$$\frac{\Delta V_0}{V_{o_{nom}}} \times 100$$

The goal was to provide a nominal voltage of 6.8 V to the load

DVo = Vomax - Vomin = rz. DIz

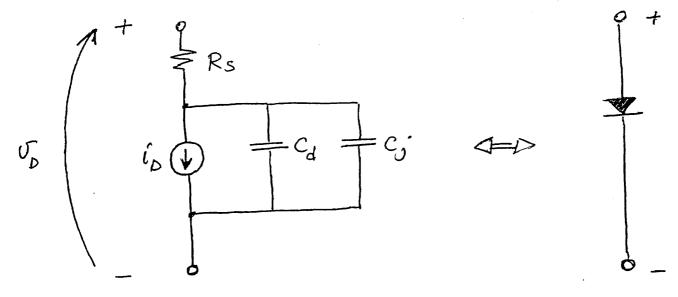
 $\Delta I_2 = \overline{I}_{2max} - \overline{I}_{2min}$

 $I_{2max} = 42 \text{ mA}$ $\begin{cases} -D \Delta I_2 \sim 33.6 \text{ mA} \end{cases}$ $I_{2min} = 8.4 \text{ mA}$

ΔVo = ΔIz· rz ~ 33.6 mA. 552 ~ 168 mV

% REGULATION = $\frac{\Delta V_0}{V_{0nom}} \cdot 100 = \frac{168 \text{ mV}}{6.8} \cdot 100 \approx 2.6\%$

NOT TOO S BAD!!



$$\hat{c}_{D} = I_{S} \left(e - 1 \right)$$

$$C_{d} = \frac{C_{T}}{V_{T}} I_{S} e^{\frac{\sqrt{D}}{2V_{T}}}$$

$$C_{J} = \frac{C_{Jo}}{\left(1 - \frac{\sqrt{D}}{D_{o}} \right)^{m}}$$

$$Cjo = \frac{A}{\sqrt{\frac{2}{qE_s} \left(\frac{NA+ND}{NA\cdot ND}\right) \phi_B}}$$

Table 3.3 SPICE DIODE MODEL PARAMETERS

(SOME OF THEM)

Model Parameter	Symbol	SPICE Name	Units	Default Value
Saturation current	$I_{\mathcal{S}}$	IS	Α	1×10^{-14}
Emission coefficient	n	N		1
Ohmic resistance	$R_{\mathcal{S}}$	RS	Ω	0
Built-in voltage	$\phi_{\mathcal{B}}$	VJ	V .	1
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M		0.5
Transit time	$ au_T$	TT	S	0
Breakdown voltage (KNEE)	V_{BR}	BV	V	∞
Reverse current at VBR (KNEE)	ĪBR	IBV	Α	1×10^{-10}

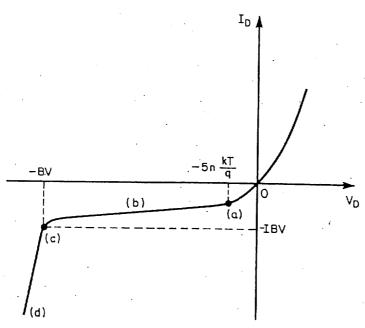


Figure 1-15 Reverse characteristic of the real diode.

From: P. ANTOGNETTI, G. MASSOBRIO

Semiconductor device modeling with SPICE

Mc Graw-Hill, New York, 1988

Robert St.

HOW TO BUILD A SPICE MODEL FOR A ZENETL

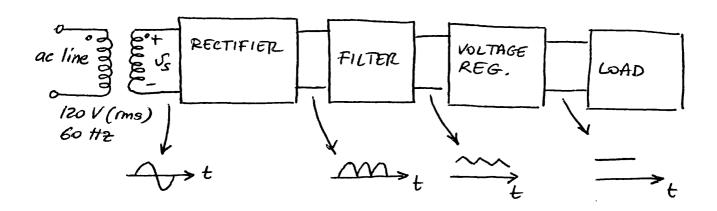
Here D_1 is an ideal diode that can be implemented in SPICE by using a very small value for n (say n = 0.01), and D_2 is a regular diode model for the forward direction of the zener (for most applications the parameters of D_2 are of little consequence).

since we do not usually use a ZENER in the forward direction we put very little attention in how DZ is modeled (-> default values are fine!!)

Fig. 3.51 Model for the zener diode. This model can be used in SPICE by defining the zener as a subcircuit. Diode D_1 is ideal and can be approximated in SPICE by using n = 0.01.

Gode Chith

· DC POWER SUPPLY DESIGN



$$\sqrt{s} \rightarrow 120 \left(\frac{Nz}{N_1}\right) \text{ volt rms}$$

The transformer besides providing the desired voltage transformation so that we have the desidered sine wave amplitude, provides electrical isolation. (-> If I have a short at the primary the primary winding will burn, but no damages to the electronic equipment attached at the secondary will occurr)

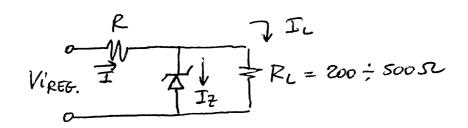
We want to design a power supply that provide a dc voltage of nominally 5V and that is able to supply up to 25 mA to the Load. The load can range from $R_L = 200 \stackrel{?}{-} 500 \text{ sc}$ We have available a zener of $V_{2 \text{ nom}} = 5.1 \text{ V}$ at $I_{2 \text{ nom}} = 20 \text{ mA}$ and $I_2 = 10 \text{ sc}$.

The maximum current that the rener can stand is $I_{zmax} = 50 \text{ mA}$ (—» the current through the sener should be at least 5 mA to be sure that we are in the constant voltage breakdown region —» Itmin = 10% Izmax = 5 mA)

lel's start our design.

The goal is to achieve the specified requirements on the load -D so let's focus on the load and proceed with the design "backward" block by block from the load to the ac line

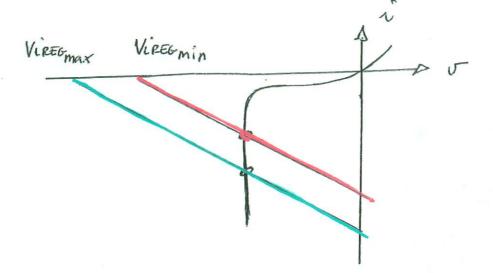
 $V_L = 5V dc.$ $I_{L_{max}} = 25 mA$



First trivial observation is that if I wanta constant voltage of 5V on the load I need a zener which has a nominal zener voltage. "close" to 5V -> we go through data sheets and we have been lucky -> we found a zener which has:

 $V_{Znom} = 5.1V$ $I_{Znom} = 20 \text{ mA}$ $\Gamma_{Z} = 105C$ ($I_{Zmax} = 50 \text{ mA}$, $I_{Zmin} = 5 \text{ mA}$)

If I want to make sure that the zener is always operating in the constant breakdown voltage region the Vires must always be relatively brigger. Than the Vanom — p at least a couple of times



Besides Vires is "fluctuating" -> (if it were not I would have not spend my time trying to regulate it !!!)

How much is "fluctuating" I do not know, but it's up to me really!!! It depends on how good I am in filtering after the rectification.

At the moment I can't say for sure, but I am reasonably confident that it shouldn't be that big deal to mantain the fluctuations within a couple of volts —D We'll cross check it later if we're able to satisfy this assumption !!!

1

VirEGmin = 10V

Viregmax - Virgnin = 2V & RIPPLE = AV

$$I = I_L + I_Z$$

0

Let's choose R!

$$I_{min} = I_{c} + I_{\overline{z}min}$$

$$5 25 mA$$

$$5 mA$$

Twe always want to be able to supply up to 25 mA to the bad

$$I_{\text{max}} = \frac{V_{\text{iest-max}} - V_{\text{Z}}}{R} = \frac{12 - 5.1}{163} \approx 42 \text{ mA}$$

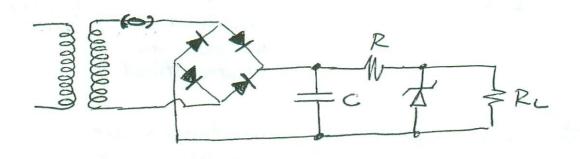
From verser point of view the worst thing that can happen is that the load get unconnected — Then all 42 mA go through the vener — The sener can stand up to 50 mA so we are safe !!!

In normal conditions only 42-25 = 17 mA goes through the zener!

$$\frac{P_R}{P_R} = \frac{V_R^2}{R} = \frac{(12 - 5.1)^2}{163} = 292 \text{ mW}$$

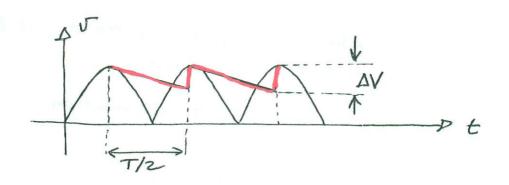
$$\frac{P_R}{P_R} = \frac{V_R^2}{R} = \frac{163}{163} = 292 \text{ mW}$$

$$\frac{P_R}{P_R} = \frac{V_R^2}{R} = \frac{163}{163} = 292 \text{ mW}$$



Let's now choose C so that we can be sure that the ripple stays below 2V (DV=ZV)

 $\Delta V = zV$



$$I = \frac{\Delta V}{\Delta t}$$
. C . $-> C = \frac{\Delta t}{\Delta V}$ $I = \frac{T/2}{\Delta V}$. $I = D$
 $C = \frac{T}{2 \cdot \Delta V}$. $I = \frac{T}{2 \cdot \Delta V}$. $I = \frac{T/2}{\Delta V}$. $I = \frac{T}{\Delta V}$. $I = \frac{T}{\Delta V}$. $I = \frac{T}{\Delta V}$. $I = \frac{T}{2 \cdot \Delta V}$. $I = \frac{T}{2$

if I take C big the discharge is slow (which is what I want!!) oversizing the capacitance C I am sure that the ripple is going to be definitely better !!!

$$C \simeq \frac{1/60}{2.2} \cdot 42 \times 10^{-3} \simeq \frac{200 \text{ nF}}{1}$$

which is rather big !!!

we need an electrolitical!!

To usually big capacitances are anything but capacitanus

$$X = j\omega L - j\frac{1}{\omega c}$$

when the frequency increases it behaves like an inductance

I pratical solution

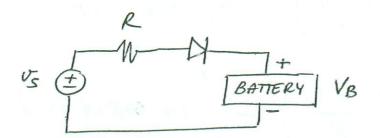
10 µF = 100 nF

at high frequency
at low
frequency
frequency
this keep the
situation under
control.

Anyway we are norking at 60 HZ so there is no problem.

Regarding the transformer we need 12V peak at the secondary so a ratio of $\frac{120.\sqrt{2}}{12} \approx 14$ is ok!

· BATTERY CHARGER



We want to design a battery charger for a battery of 12 Vdc that supplies 100 mAde

$$\frac{1}{I_{brms}} = \frac{1}{\pi} \left(\frac{V_{P} - V_{B}}{R} \right)^{2} - \int_{0}^{\infty} \cos^{2}\varphi \, d\varphi = \frac{1}{\pi} \left(\frac{V_{P} - V_{B}}{R} \right)^{2} \cdot \frac{1}{2} \int_{0}^{\infty} (1 + \cos^{2}\varphi \, d\varphi)$$

We want:

$$V_p = 24$$
 $\rightarrow \frac{V_B}{V_p} = \frac{1}{2}$ $\rightarrow \frac{V_B}{V_p} = \frac{1}{2}$ $\rightarrow \frac{V_B}{V_p} = \frac{1}{2}$ $\rightarrow \frac{1}{2}$

$$\int_{0}^{\pi/3} d\varphi + \int_{0}^{\pi/3} \cos 2\varphi \, d\varphi = \frac{\pi}{3} + \int_{0}^{\frac{1}{2}} \cos x \, dx = 0$$

$$2\varphi = x$$

$$d\varphi = \frac{dx}{2}$$

$$= \frac{\pi}{3} + \frac{1}{2} \left[\sin x \right]^{\pi/3} = \frac{\pi}{3} + \frac{1}{2} \left[\frac{\cancel{3}}{2} - 0 \right] =$$

$$=\frac{76}{3}+\frac{\sqrt{3}}{4}$$

$$|D^{2} = \frac{1}{\pi} \left(\frac{\pi}{3} + \sqrt{3} \right) \cdot \frac{1}{2} \left(\frac{12}{R^{2}} \right) - P$$

$$|O^{2} = 0.24 \cdot \frac{144}{R^{2}} - P \quad R \simeq 59 \quad \Omega$$

PIV on the diode

$$\begin{array}{rcl}
\text{Topenk} &=& \frac{24-12}{55} = \\
& & \cong 218 \text{ mA} \\
12+24=36
\end{array}$$

SPECIAL TYPES OF DIODES

· Schottky barrier diodes



The junction formed by a metal and a doped semiconductor can be either rectifying or ohmic. (because of the difference in carrier concentrations in the two materials, a potential barrier exists -D in ohmic contacts care is taken to eliminate the effect of the barrier)

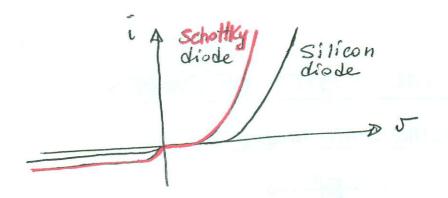
Schottky diodes are formed bringing together a metal (typically aluminium or platinum) and an n-type semiconductor material (silicon).

in schottky diodes the current is conducted by majority carriers (-> this means that there is no charge-storage effect due to the minority carriers -> a schottky diode can be switched on- off faster)

The reason why the current is conducted by majority carriers is that in the metal

There are available numerous electrons!

The forward voltage drop of schottky dioles is smaller 0.3 = 0.5 V, and the reverse saturation current is higher



VARACTOR



A varactor is a diode specifically manufactured to be used as voltage variable capacitor.

A biased projunction exhibts a certain capacitance that is function of the applied voltage
$$Cj = \frac{Cjo}{\left(1 + \frac{V_b}{P_B}\right)^m}$$

$$C_d = \frac{\tau_T}{V_T} e^{J_D/\eta V_T}$$

usually they are used with a reverse bias !!!

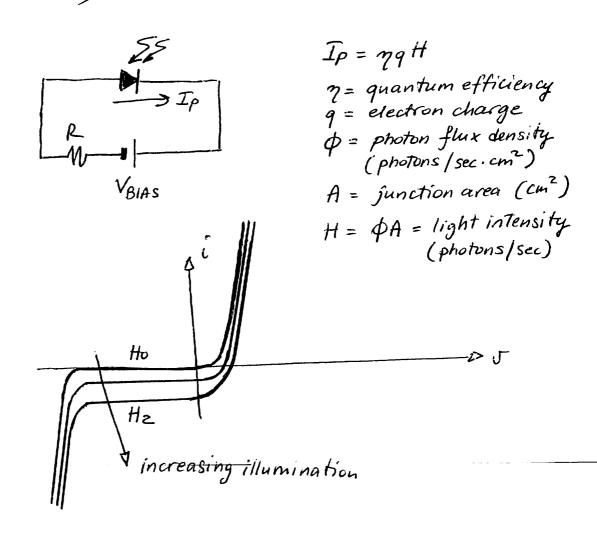
-D no current flowing through the device
and I can get a bigger DC enlarging the
depletion region (-) rather than trying to shrink
it applying a forward bias)

· Photodiodes

If a photons impacting the junction cause covalent bonds to break, and thus electron-hole pairs are generated (—D which induce current)

Photodiodes are usually fabricated using GaAs.

A photodiode converts light to electrical energy (—D using the photodiode farmard bias we have a solar-cell —D photodiodes for Solar cells are usually fabricated from rather cheap silicon)



common application - D optical receivers

Light emitting diodes (LEDs)



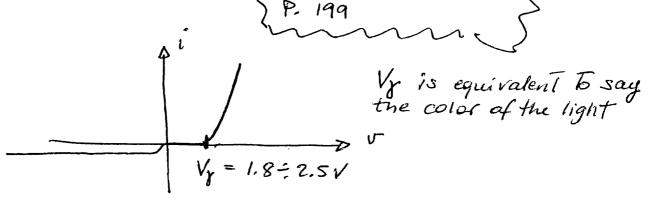
The LED performs the inverse of the function of the photodiodes (electric energy)

It converts a forward current into light.

The light emitted by a LED is proportional to the number of recombinations that take place and therefore is proportional to the current in the diode.

When an electron fall from the conduction band into a hole give up energy in the form of light !!

GaAs emits light waves at a wavelength near the infrared band. To produce light in the visible range, GaP (gallium-phosphide) must be mixed with the GaAs. >>ERROR ON TEXTBOOK?



LED are used in forward-bias!

LASER = LED designed so as to produce coherent light

(very narrow bandwidth)

OPTOISOLATOR =

